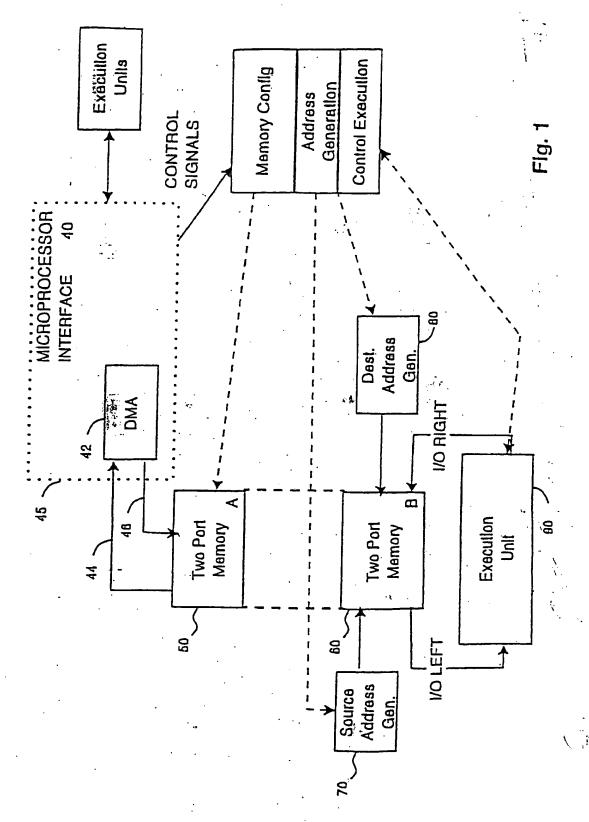


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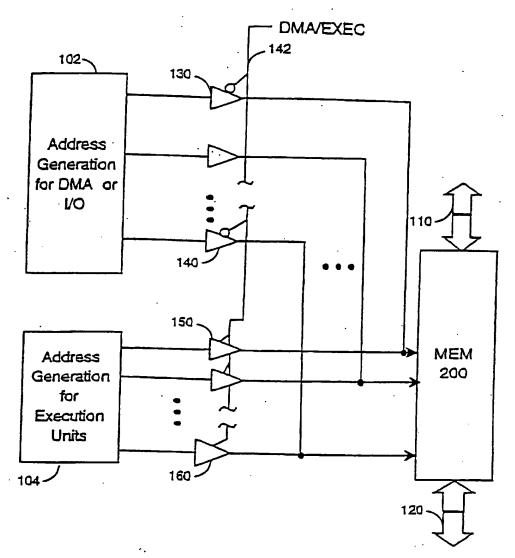


FIG. 2

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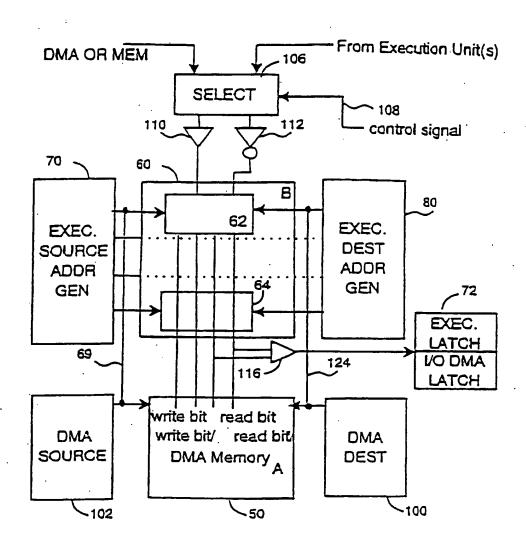
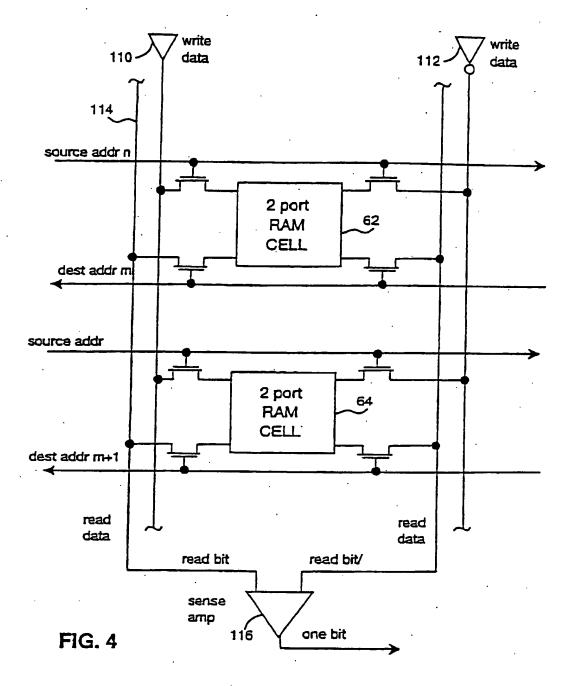


Fig. 3

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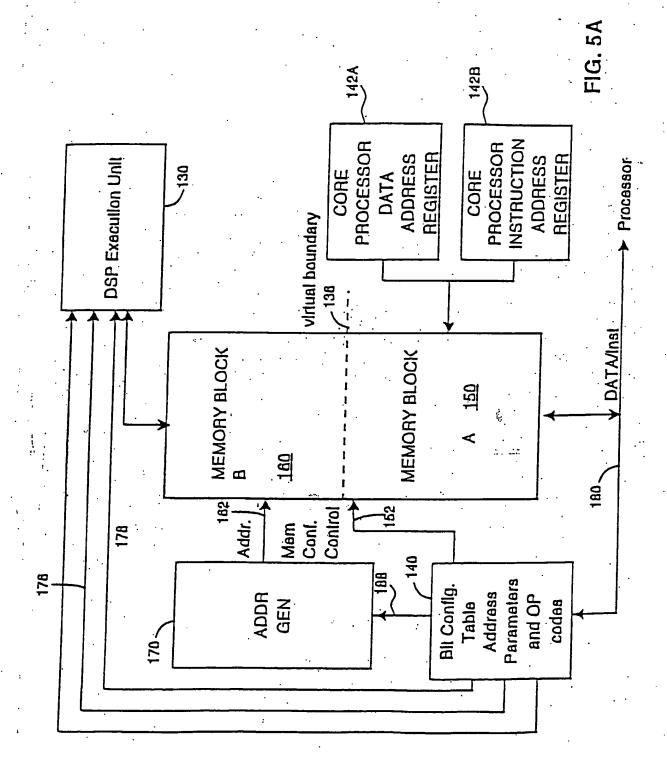
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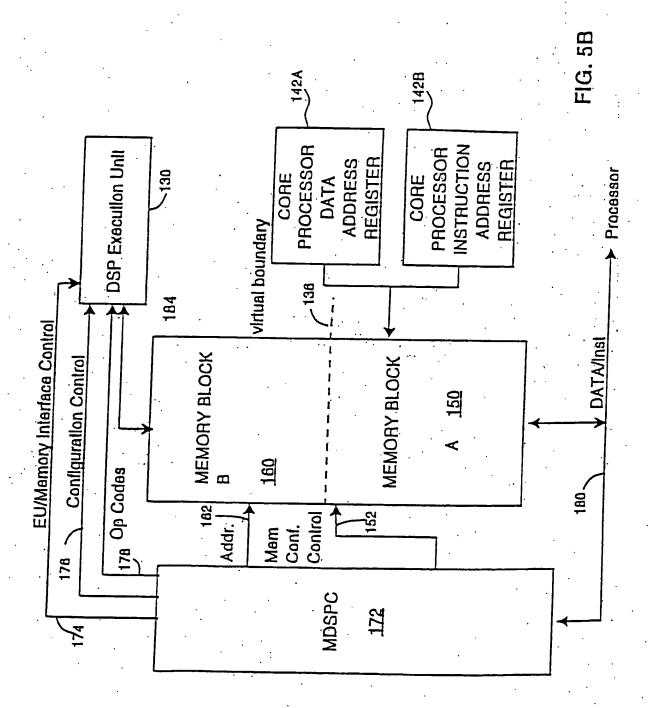
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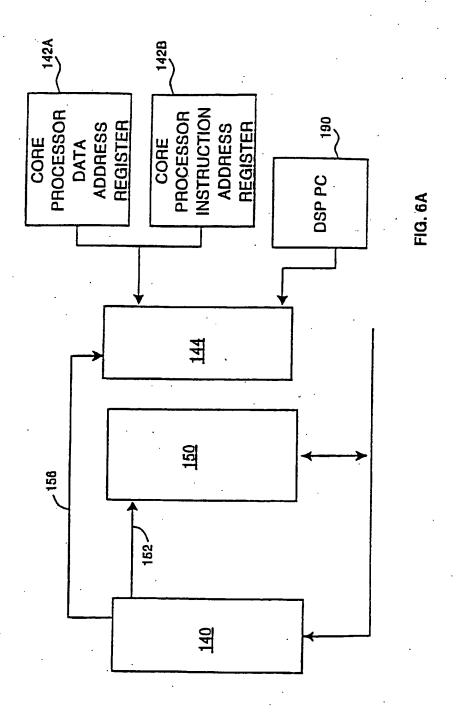
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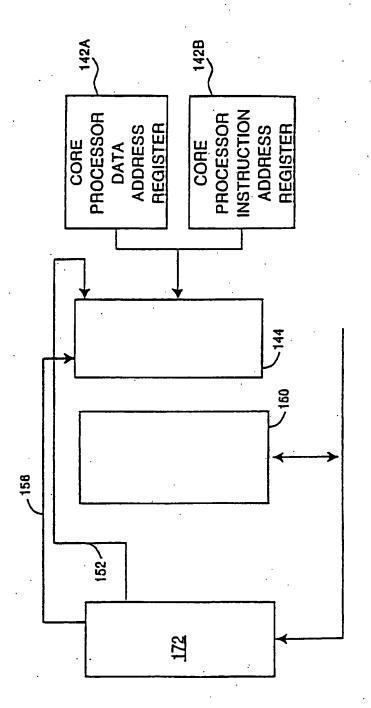


FIG. 6B



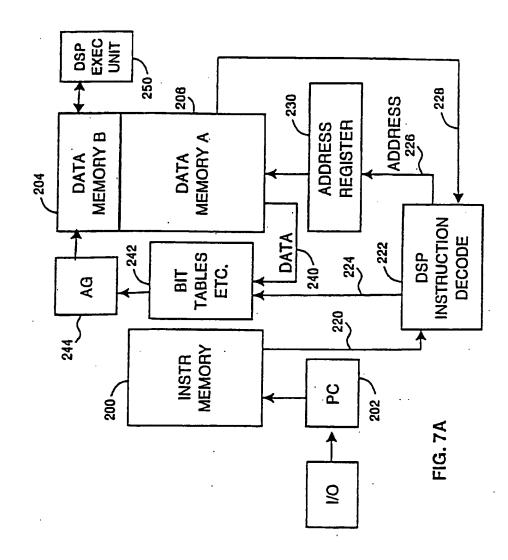
Inventors: Brent Lebeck et al

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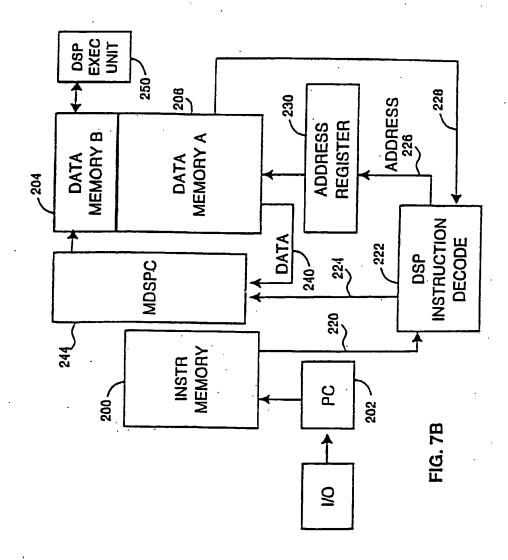
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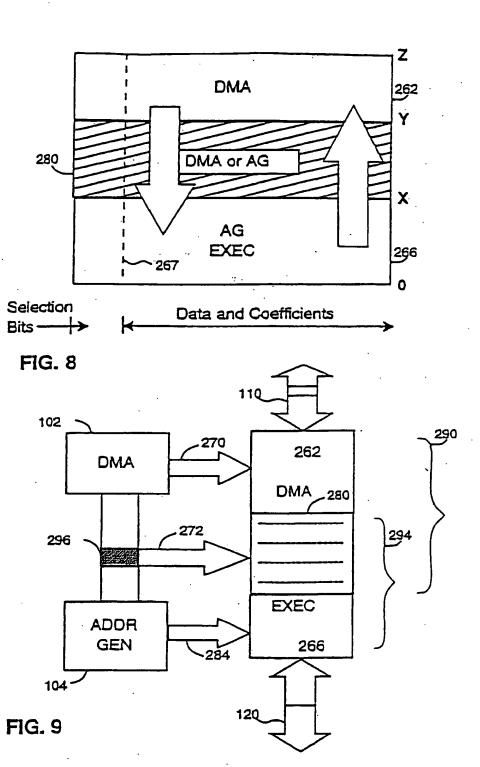
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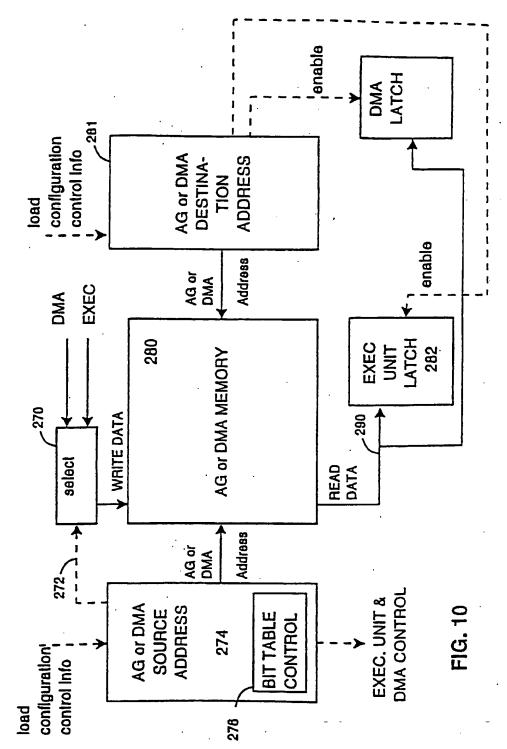
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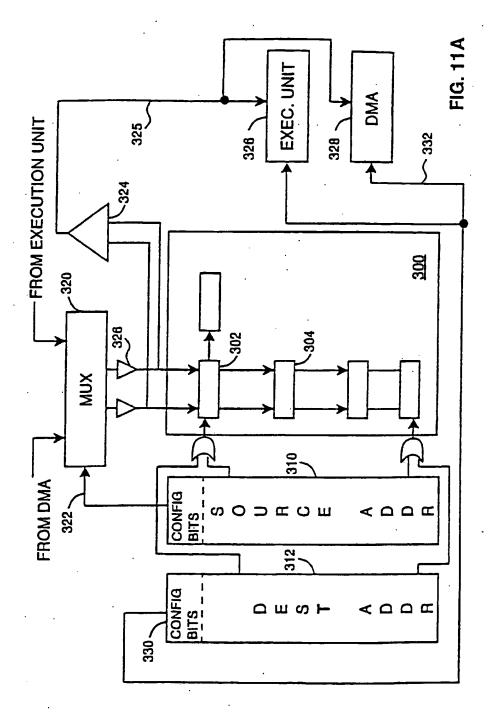
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. T4	DEST. EXEC	DMA selection
T3	SOURCE	dest. address read control exec. selection
T2	SOURCE EXEC	
F	SOURCE	generator address write control exec selection address latch
•	MEMORY ACTIVITY	ADDRESS & CONTROL GENERATION



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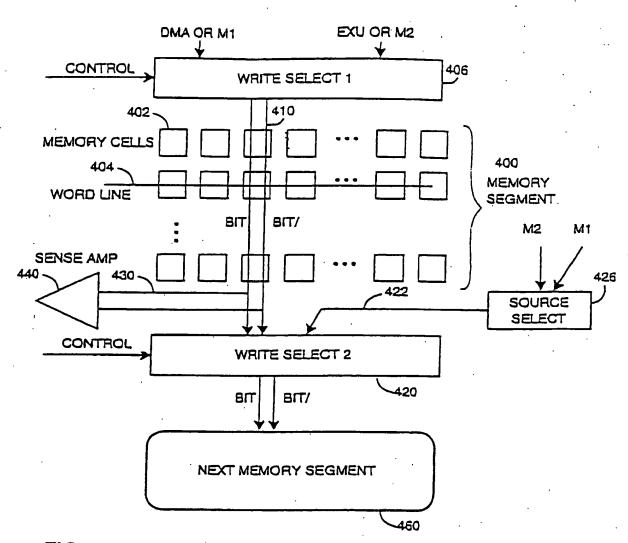
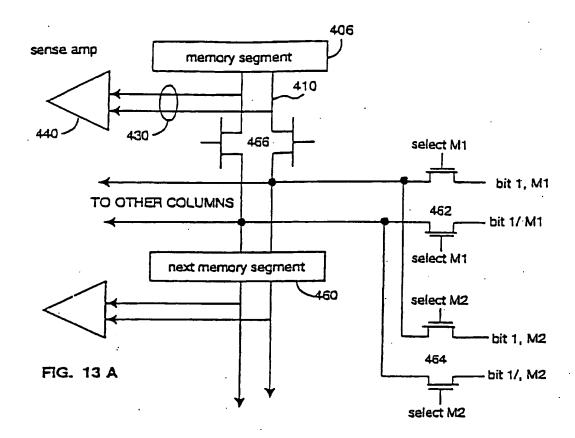
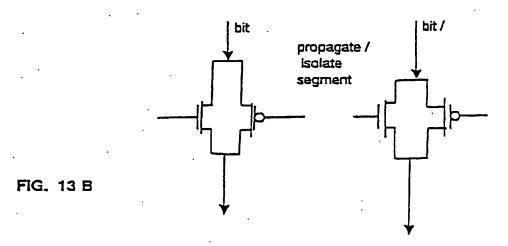


FIG. 12



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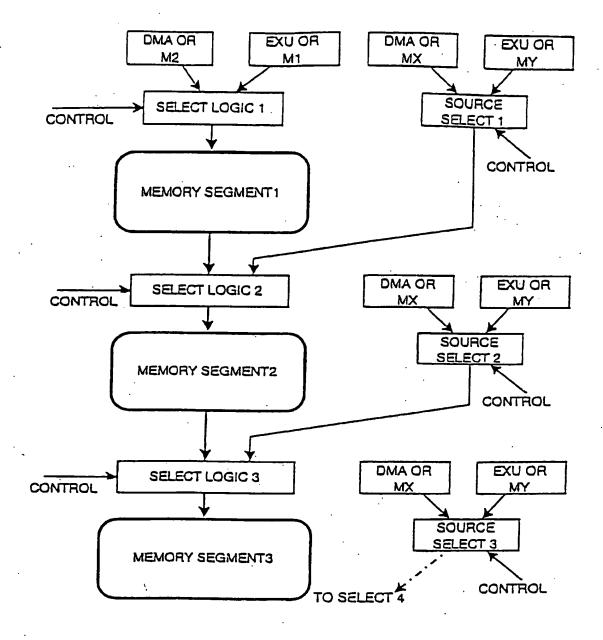


FIG. 14



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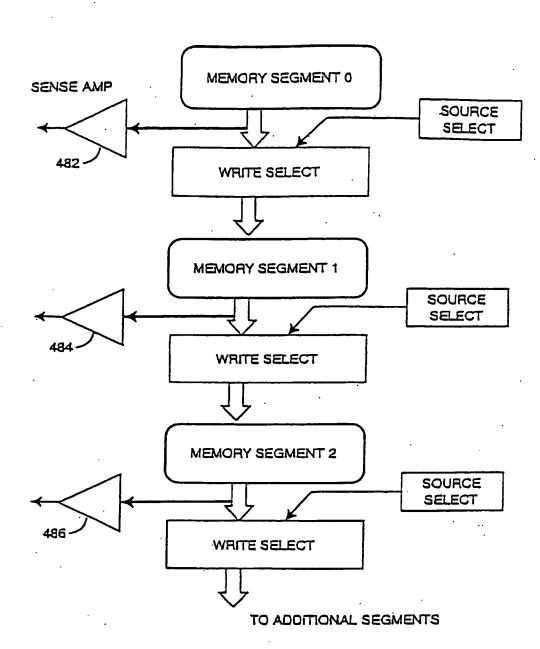
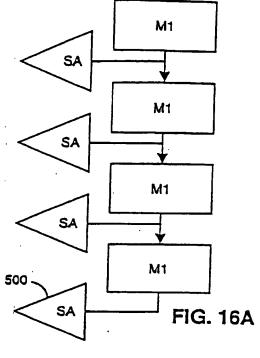
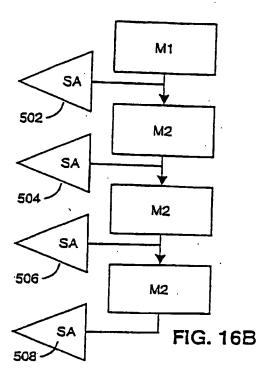


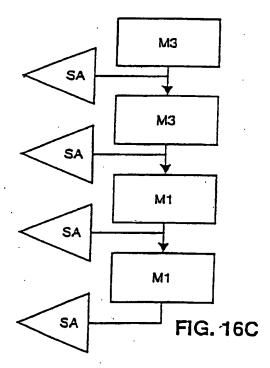
FIG. 15

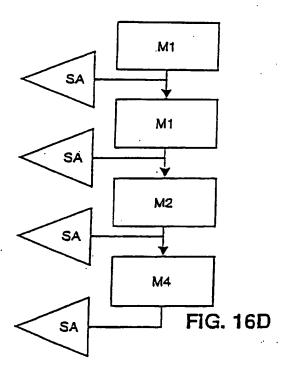


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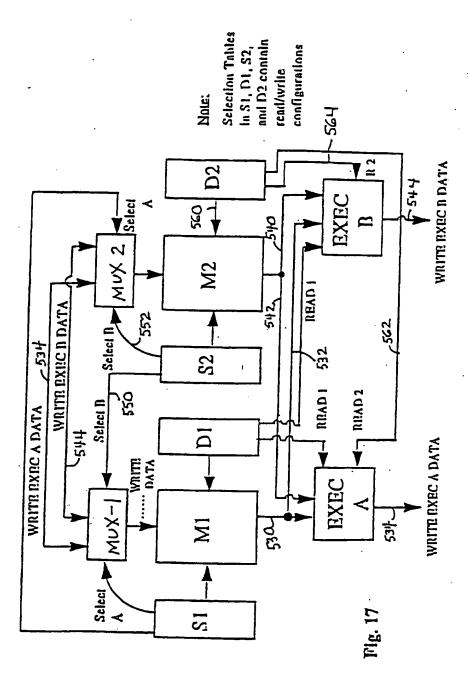








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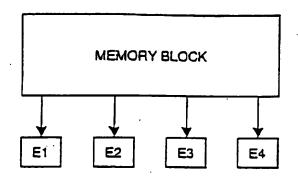


FIG. 18A

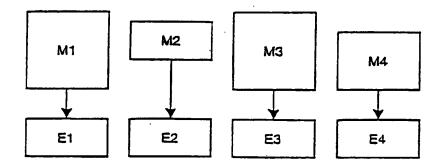


FIG. 18B

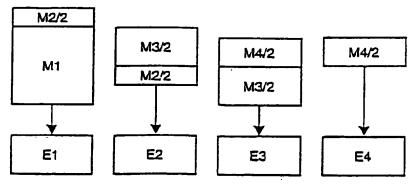


FIG. 18C



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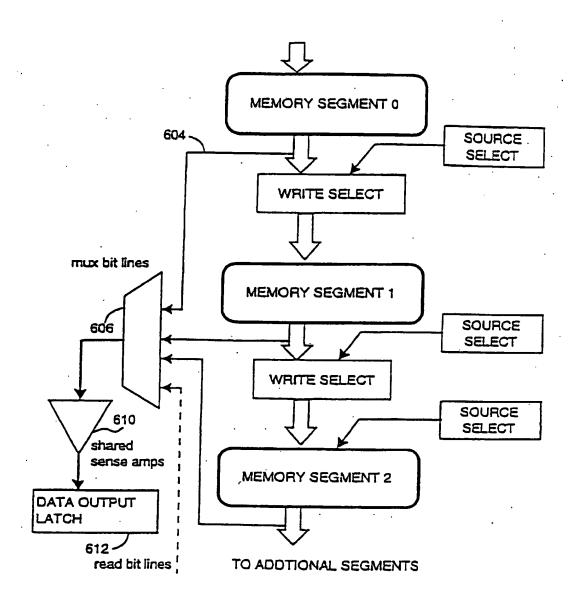


FIG. 19



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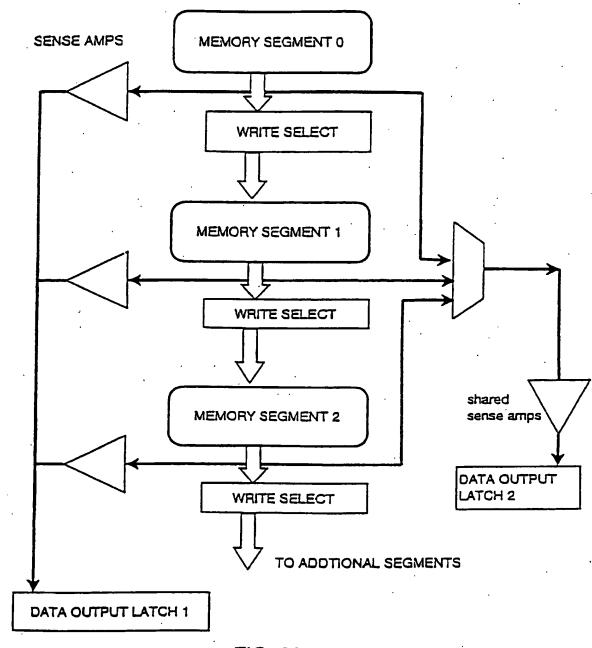
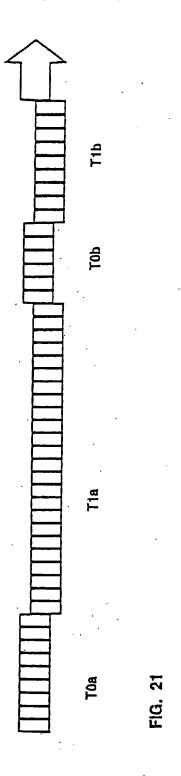


FIG. 20

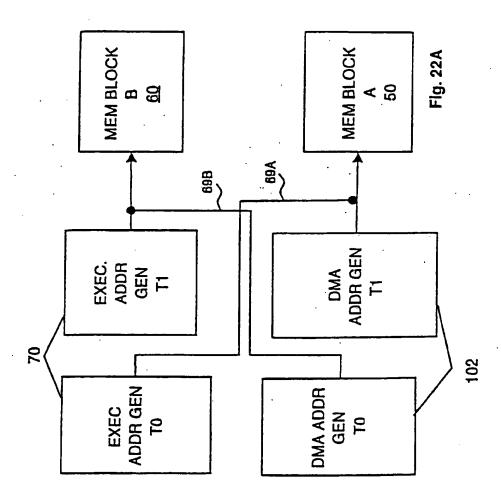


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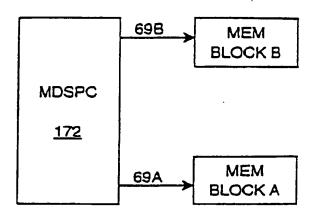


FIG. 22B

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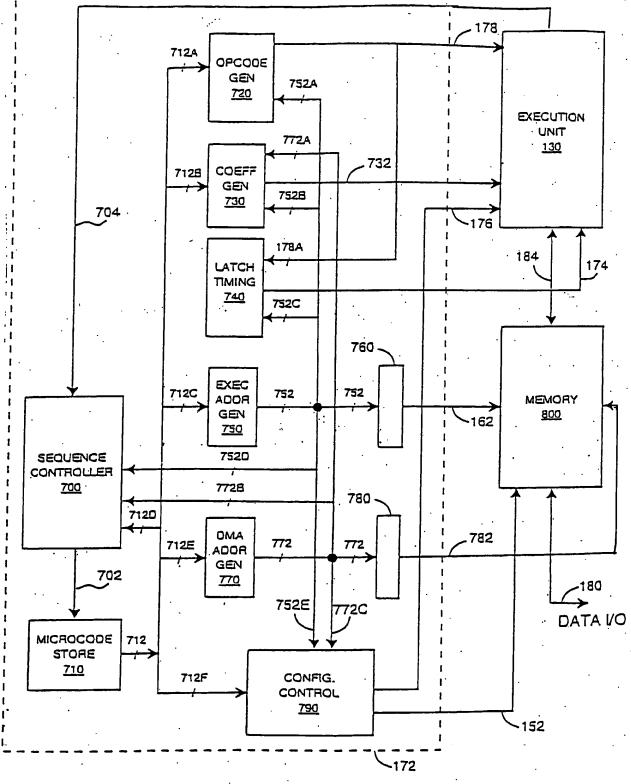


FIG. 23A



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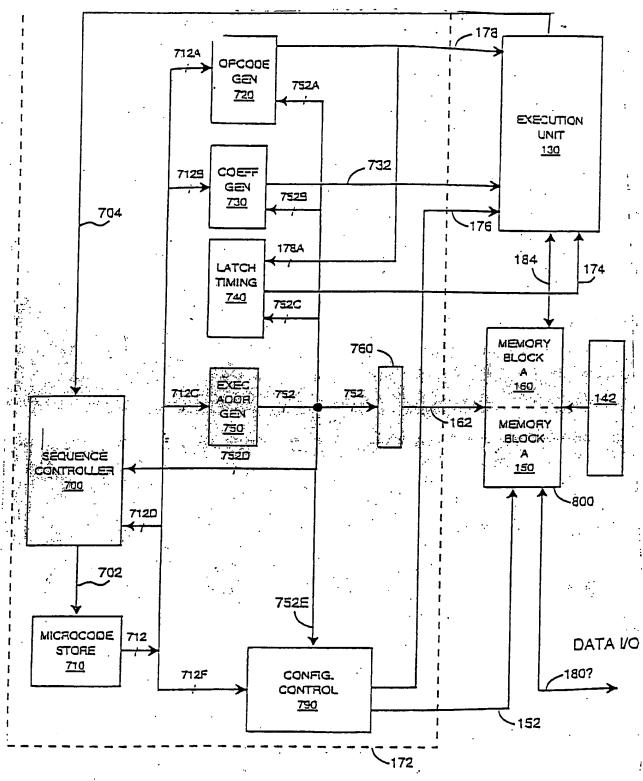


FIG. 23B



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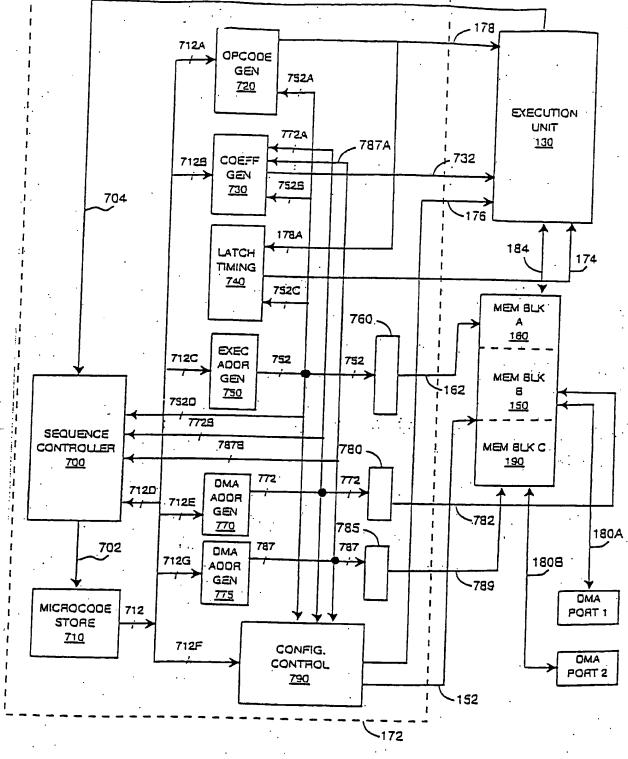


FIG. 23C



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	ADORESS	FUNCTION
	0x710	FFT RADIX 2
	0×905	FIR FILTER
	0x2100	CONVOLUTION
Ĺ		

FIG. 24A

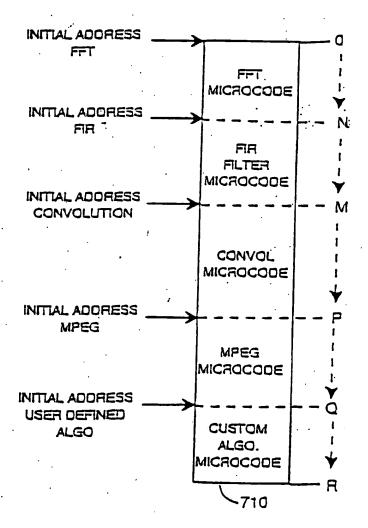


FIG. 24B



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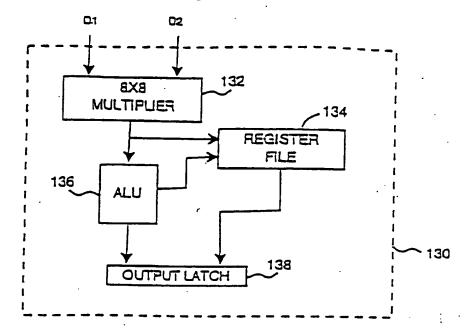


FIG. 25

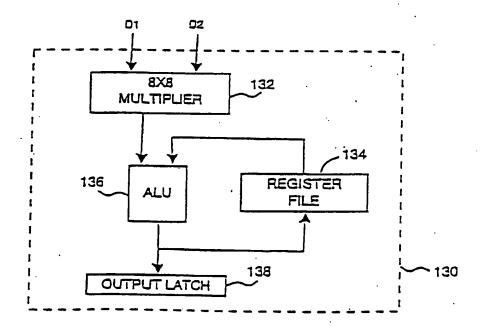
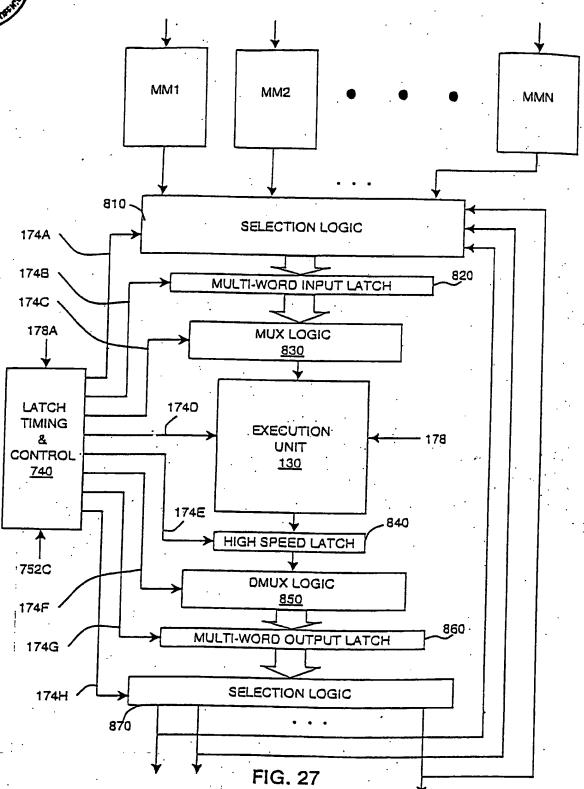


FIG. 26

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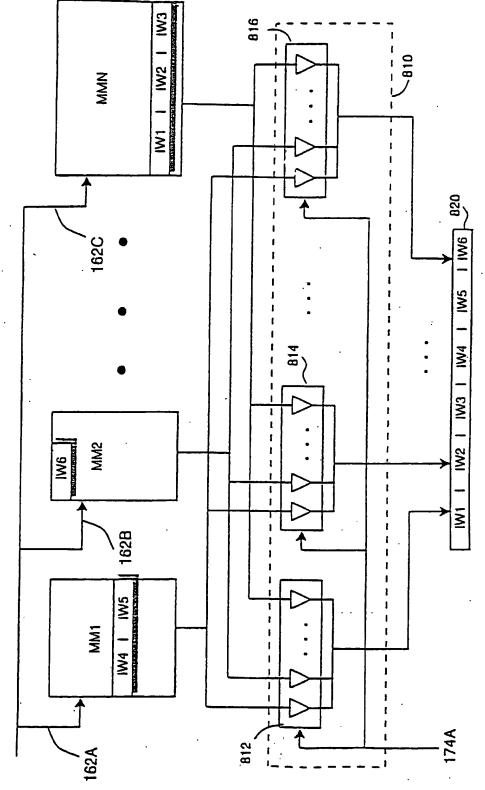


FIG. 28

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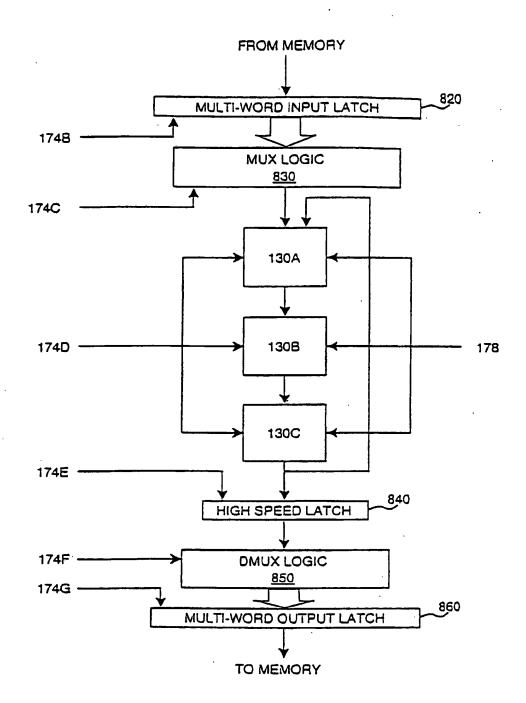
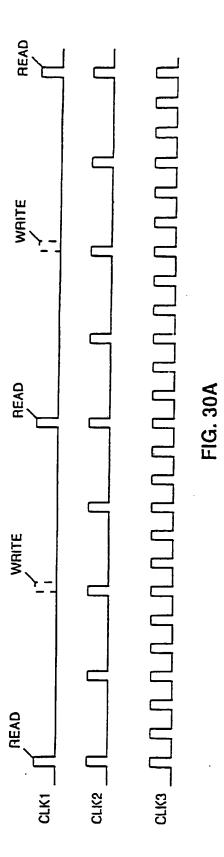
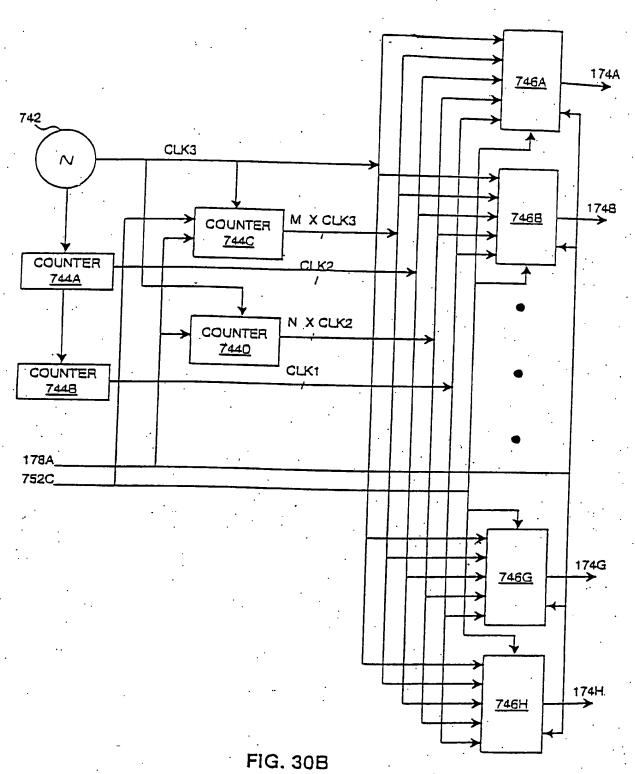


FIG. 29



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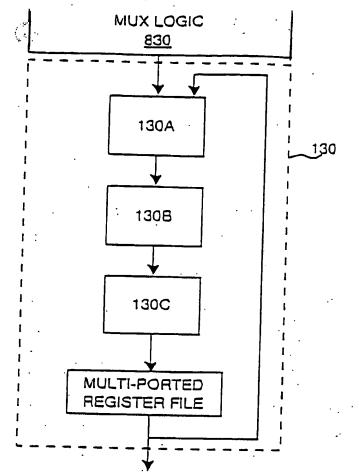


FIG. 31

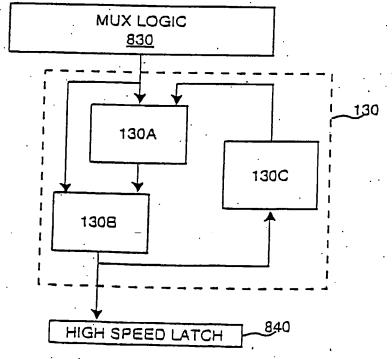


FIG. 32



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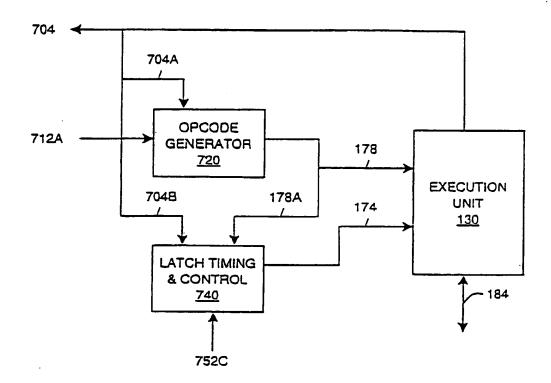


FIG. 33



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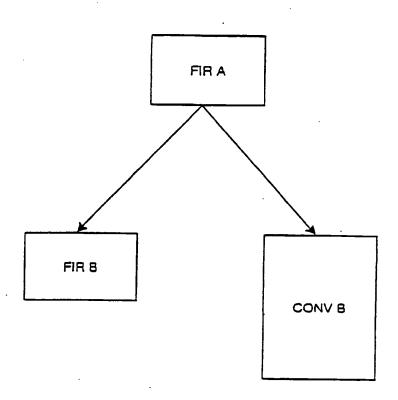


FIG. 34

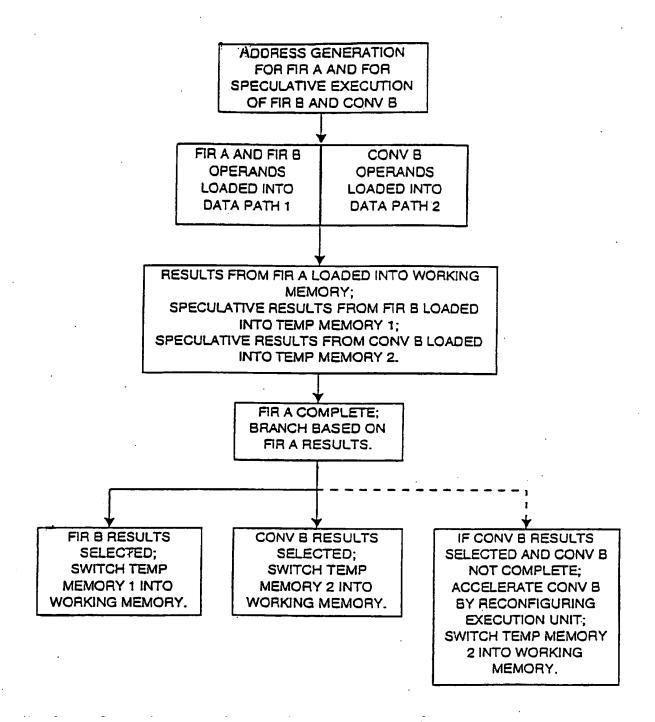


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WORKING MEMORY	
TEMP MEMORY 1	1
TEMP MEMORY 2	
	- 7
	1
•	1
•	i
	1
•	i
	ł
TEMP MEMORY N	1
	ı

FIG. 36